Multiprocessor Architectures and Programming

Overview

With the advent of low-cost off-the-shelf multicore computers in the market, multiprocessing has shifted from using traditional cluster computing to desktop computers. This course will cover the fundamentals behind the design and use of these multiprocessors. They comprise of instruction level parallelism, multithreading, shared memory, cache coherence protocols, non-uniform memory access (NUMA) and interconnection network architectures. Designing and scheduling parallel algorithms will be presented for efficient use of the multiple cores on these computers. Further acceleration can be realized through heterogeneous design by connecting multiple cores with accelerators such as GPU and FPGA. The architecture and programming of GPU-based heterogeneous multiprocessors will also be covered. The course will consist of projects and discussion of results on the real implementation of scientific benchmark applications using the multicore machines or architecture simulators.

Modules	**A: Multiprocessor Architectures : 16-20 December** **B: GPU and CUDA Programming : 21-23 December** **Number of participants for the course will be limited to 50 (fifty).**
You Should Attend If…	▪ you are a Computer Scientist, an Electronics engineer or a researcher in the areas of Multiprocessor Architecture and Programming. ▪ you are a student or faculty from academic/research institutions interested in Modern CPU, GPU Architectures
Fees	The participation fees for taking the course is as follows: **Participants from abroad : US $500** **Industry/ Research Organizations: Rs. 6000** **Academic Institutions: For Faculty Members: 4000;** **Students: Rs. 2000** ▪ The above fee include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24hr free internet facility. The participants will be provided with accommodation on payment basis.

The Faculty

Prof. L.N. Bhuyan: Laxmi Narayan Bhuyan is a Distinguished Professor of CSE Department at the University of California, Riverside (UCR). Dr. Bhuyan is a Fellow of the IEEE, a Fellow of the ACM, a Fellow of the AAAS, and a Fellow of the WIF. He has also been named as an ISI Highly Cited Researcher in Computer Science. Dr. Bhuyan served as the Editor-in-Chief of the IEEE TPDS. He is a past Editor of the IEEE TC, JPDC, and Parallel Computing Journal.

Dr. A. Nanda: Ashwini Nanda is the Founder and CEO of HPC Links Pvt. Ltd. For over twenty years, Dr. Nanda has been involved in R&D of HPC systems and applications in both India and the US. At CRL, India, he led the development of the Eka system that became Asia's fastest supercomputer in 2007. Prior to that, at IBM TJ Watson Research Center, NY, he led the development of Cell processor based system and software technologies resulting in a new line of server product offerings from IBM, and the world's first Petaflop machine, Roadrunner, at Los Alamos National Labs. He is a Fellow of the IEEE.

Dr. Manoranjan Satpathy is an Associate Professor of Computer Science at Indian Institute of Technology, Bhubaneswar. His research interests are Formal Modelling, and Testing/ verification of software and hardware systems. Earlier he has worked as a Staff Researcher at General Motors Research Lab at Bangalore.

Venue:

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Account Details

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